Aerosol-Jet Printed Thin Film Transistors

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SUMMARY

Thin film transistors are at the heart of integrated circuits. Modern computer processor chips can contain more than 2 billion transistors. Such chips are currently fabricated by expensive lithography processes and fabrication facilities can cost more than one billion US dollars. In a future era of cheap, disposable electronics such cost structures will not be practical. Printed electronics however offers a potential solution that can reduce costs and produce truly disposable electronics. Many printing technologies and materials are being developed to meet this need and most efforts focus on printing passive electronic components such as conductors, resistors, capacitors, and antenna. However, to create integrated circuits, active devices are needed. So far, printed active components, such as transistors, diodes, and sensors, have been lagging, mainly due to poor material performance but also deficiencies in the printing technologies. In this paper, the Optomec Aerosol-Jet printing system is introduced as a solution to integrated circuit printing.

INTRODUCTION

Aerosol Jet printing is a maskless additive manufacturing solution that reduces the overall size of electronic systems by using nanomaterials to produce fine feature circuitry and embedded components. The resulting functional electronics can have line widths and pattern features below 10 microns, and as large as several millimeters. The system can directly deposit a wide range of commercial and custom electronic materials, including conductor, insulator and adhesive formulations onto virtually any substrate. The support of nanomaterials allows for low-temperature processing and ultra-thin layers where needed.

ABOUT AEROSOL JET PRINTING of TFTs

Optomec has recently teamed up with Brewer Science, the University of Massachusetts, and the University of Minnesota to develop all-printed, high performance thin film transistor circuits. This teaming relationship brings together experts in materials, device physics, printing, and circuit design. Brewer Science's expertise is in developing high-performance single-walled carbon nanotube (SWCNT) ink formulations for printable semiconductor and conductor devices. The performance of SWCNTs can potentially exceed that of crystal silicon, but to date the commercial ink formulations have suffered from impurities and contamination. Brewer Science is developing a novel technology for purifying CNT solutions, with resulting enhancement in electrical performance. The University of Minnesota has expertise in organic electronics and they have specifically developed an enabling gate dielectric material for printed transistors. Standard printable dielectric materials have low dielectric constants which result in high device operation voltage and limited output currents. The UMN ion-gel dielectrics have a specific capacitance of approximately 10 $\mu F/cm^2$ which results in very low operating voltage and high current output for organic field effect transistors. The University of Massachusetts-Lowel laboratory specializes in RF electronics and has recently benchmarked an Aerosol Jet printed CNT transistor operating at 5 GHz.

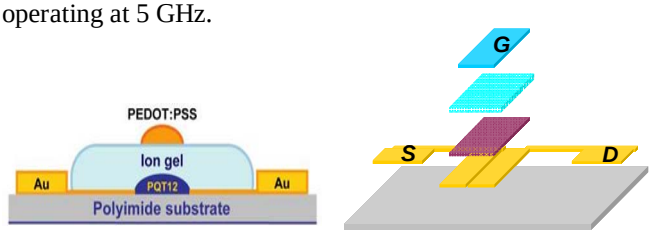

Figure 1: Schematic diagram of top gated field effect transistor. The drain source electrodes are printed with either gold nanoparticle ink (UT Dots, Inc.) or conductive polymer PEDOT:PSS (H.C. Stark). Various semiconductors have been used including P3HT (Rieke Metals, Inc), PQT12, and F8T2(American Dye Source, Inc.), SW CNTs (Brewer Science, Inc.). The gate dielectric is printable ionic gel (U. of Minnesota). The top gate is conductive polymer.

The schematic of a top-gated field effect transistor is shown in Figure 1. The device typically consists of four distinct materials printed into four separate layers. The first layer consists of drain and source electrodes printed with high conductivity conductor material. Gold inks are typically selected for this layer because the chemical inertness makes it compatible with the other materials. The high work function of gold also enhances the performance of TFTs. Other conductors, such as PEDOT:PSS, can also be used for the electrode layer depending on level of optical transparency and conductivity desired. The channel length, or gap, between the drain-source electrodes is between 5 and 50 microns typically. Smaller channel lengths are generally desired due to increased frequency response and current output. However, SWCNT materials often contain impurities that negatively effect performance at the small size scale, so in this case large channels are preferred. The semiconductor is printed in the channel between drain-source electrodes. Organic semiconductors such as PQT12, P3HT, and F8T2 have been evaluated as well as formulations of SWCNTs. An insulating dielectric, printed over the channel, serves to insulate the gate electrode from the channel. The University of Minnesota's ion gel

dielectric has an exceedingly high dielectric constant (~10 microFarad/cm2) which gives rise to low voltage operation and high current output. Finally, the top gate electrode is typically a conductive polymer (PEDOT:PSS), but other compatible conductors could also be used. The PEDOT:PSS is conductive after air-drying, whereas metal nanoparticle inks require thermal sintering at temperatures ranging from 120C to 250C for 30 minutes.

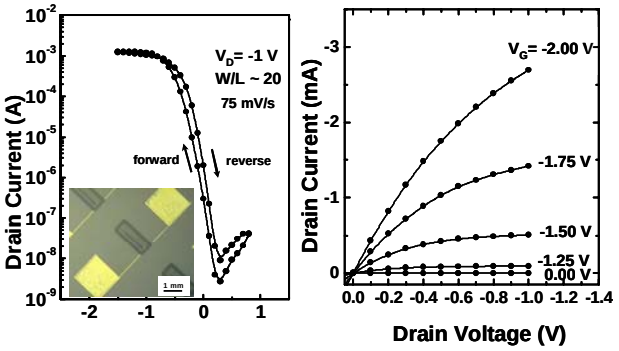

Figure 2: I/V characteristic of an all-printed organic field effect transistor. The device mobility is typically 3 cm2/Vs, the on/off ratio ~105, and threshold voltage ~0.05 V. The optical image shows a single device printed on flexible PET.

Typical I/V curves of an AJ-printed organic field effect transistor are shown in Figure 2[1,2]. The device utilizes gold for the drain-source electrodes, PQT12 for the semiconducting channel, ion gel for the gate dielectric, and PEDOT:PSS for the gate electrode. The p-type device has an on current of 1 mA an on/off ratio of ~10^5, a threshold voltage of ~0.05. The mobility, calculated by the small signal transconductance, is 3 cm^2/Vs. These values generally exceed the performance obtained by other printing techniques. FET devices have been printed on PET, PEN, and polyimide film as well as glass and silicon wafer. The switching speeds exceed 10 kHz for the organic semiconductor devices, with the main limitation being the roll off of the ion gel dielectric constant as the frequency increases. The devices have been shown to be stable for months when stored under ambient conditions. However, the continuous operation lifetime is currently limited a few days. The exact mechanisms for the lifetime degradation are not know, but it is believed that overcoating the FET with an impermeable encapsulant will inhibit environmental degradation.

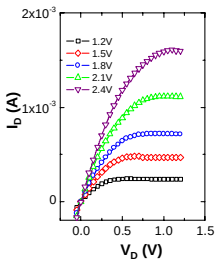

Figure 3: Output characteristics of an ion-gel gated carbon nanotube FET. Hole mobility up to 67 cm2/Vs, electron mobility of 56 cm2/Vs, and on/off ratios of 105 have been achieved.

The I/V curve on an AJ-printed CNT transistor is shown in Figure 3. The majority carrier is n-type in this case, but p-type transistors have also been fabricated. Similar to the organic transistors, the on-current is ~1mA, the on/off ratio is 10^5, and the threshold voltage is near zero. However, the mobility is more than 10 times higher for the SWCNT semiconductors compared to the organic semiconductors. Since the theoretical mobility for the carbon nanotubes is very high (~100,000 cm^2/Vs), we expect additional performance enhancements will be achieved with improved inks and printing techniques. In contrast to the organic FETs, the printed SWCNT transistor is observed to be stable for many days under continuous operation,. The SWCNT transistor has been shown to operate at up to 5 GHz[3].

Since the AJ printing technique is widely flexible with respect to materials, printed feature geometry, and complexity of printed features, it is an ideal for prototyping complex integrated circuits. As noted previously, passive elements such as resistors, capacitor, inductors can be printed[4]. Insulating materials can also be printed to electrically isolate various layers of a circuit. Complex integrated circuits will require combining the passive and active device printing. However, the printing of integrated circuits requires careful consideration of materials compatibility both with the printing system and with other materials in the circuit, software automation, and system optimization. Each potential material is screened to evaluate atomization ability, printability, process conditions, and finally the electrical and mechanical characteristics.

To facilitate the screening, disposable material reservoirs have been developed so that the material can be easily inserted and removed from the atomizer. Separate material reservoirs also mitigate the potential cross contamination that can arise when using the same equipment for multiple materials. As each material is evaluated a log of preferred process parameters are retained for future use. The software deals with each material as an individual layer to be printed. For example a gold ink would be printed as the first layer of a transistor circuit. A semiconductor ink would be the second layer and would be printed only in the channel region. Each material layer in the software contains specific process information, such as flow rates and substrate temperature for that material, as well as a toolpath for directing the placement on the substrate. When printing a multilayer circuit, the process flow consists of only a few steps: i) load material #1, ii) print material #1, iii) process material #1, iv) load material #2, and so forth until the final layer is reached.

To illustrate this process, Figure 4 shows a moderately complicated 5-stage ring oscillator circuit. Each element of the circuit consists of a resistor-loaded transistor inverter, a resistor printed between the power supply and the transistor drain serves to invert the voltage as the transistor switches. The overall circuit consists of six discrete inverters connect from end-to-end. The output from each inverter drives the input of the subsequent inverter. The output of the fifth

stage is connected to the input of the first stage to form a connected ring. The sixth inverter is only used as an output buffer. The connection from the fifth inverter to the first must cross over the grounded source electrode. An insulator is printed at the crossover location to insulate the traces. Overall, this circuit can be reduced to five material printing steps: electrode and interconnect conductor, semiconductor, gate dielectric, crossover dielectric, and gate conductor. Each material is typically processed before proceeding to the next. Ideally, the materials would be processed without removing the substrate from the printer and multiple atomizers would be incorporated so that material would not have to be manually switched. In this case, all aspect of printing and processing would be under software control, i.e. completely automated printing of complex circuits.

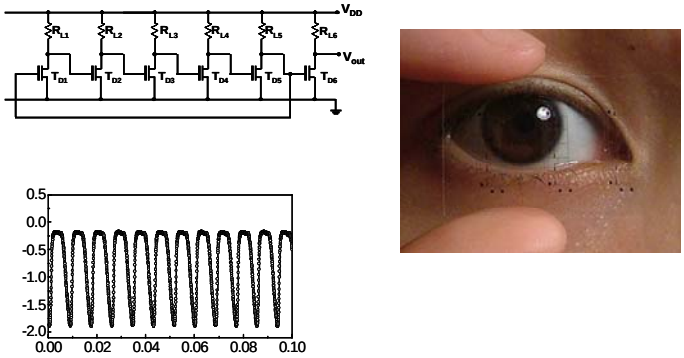

Figure 4: Circuit diagram of a five stage, resistor-loaded ring oscillator. Each transistor has a channel length of 5 um and a width/length ratio of 20. The load resistor is 5 kOhm. The circuit begins to oscillate when VDD ~ -0.45V and a frequency of 117 Hz is achieved when VDD = -3.0 V. The optical image demonstrates that the device is nearly transparent when printed on clear PET.

The output performance of the ring oscillator is also shown in Figure 4. The circuit begins to oscillate spontaneously when a threshold voltage is supplied. The oscillation frequency depends on several factors including the magnitude of voltage supply, the resistor values, and the overall geometrical circuit design and is tunable over the frequency range from 2 Hz to 117 Hz. Oscillators are one building block analog and digital circuitry. Other building blocks would include logic gates, memory elements, ALU, and input/output devices. Demonstrated printing of all these building blocks have either been accomplished or are planned for the near future.[5]

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